AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. **(Currently Amended)** A content addressable memory (CAM) cell having a plurality of 6T ternary memory cells in a fabricated semiconductor material, each ~~ternary~~ half of the CAM cell comprising:

an equal number of transistors of a p-type and an n-type, the p-type transistors being formed in a n-well region and the n-type transistors being formed in a p-well region of said semiconductor material, the p-wells being separated from the n-wells by at most one p+ to n+ region spacing, the transistors being interconnected to form said half ~~ternary~~ CAM cell and wherein the interconnections between the half CAM cell are restricted to a first group of conductive layers and connections between said CAM cell and CAM signal lines external to said CAM cell are formed in a second group of conductive layers.

2. **(Currently Amended)** A CAM as defined in claim 1, said ~~external~~CAM signal lines external to said CAM cell ~~including~~ include a search line, matchline, bitline and word line.

3. **(Original)** A CAM as defined in claim 2, said search line being formed in a third metal layer.

4. **(Original)** A CAM as defined in claim 3, said matchline and wordline being formed in a fourth metal layer.

5. **(Currently Amended)** A CAM as defined in claim 1, said ~~bit line~~bitline being formed in a fifth metal layer.

6. **(Currently Amended)** A CAM as defined in claim 1, said ~~silicon layer~~conductive layers ~~including~~ include at least one polysilicon layer.

7. **(Currently Amended)** A content addressable memory (CAM), comprising:

(a) a plurality of ~~6T~~ half ternary CAM cells each having at least one 6T ternary memory cell and an equal number of transistors of a p-type and an n-type, the p-type transistors being formed in a first well region and the n-type transistors being formed in a second well region of a semiconductor material, the ~~p-wells~~first well region being separated from the ~~n-wells~~second well region by at most one p+ to n+ region spacing, the transistors being interconnected to form said half ternary CAM cell and wherein the interconnections are restricted to a silicon layer and a first metal layer;

(b) power lines formed in a second metal layer and coupled to said cells;

(c) a plurality of search lines formed in a third metal layer;

(d) a plurality of wordlines and matchlines formed in a fourth metal layer; and

(e) a plurality of bitlines formed in a fifth metal layer.